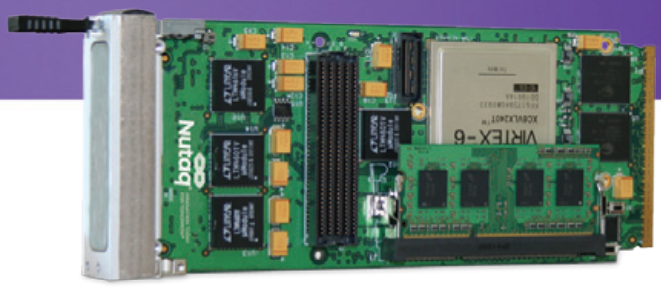
Nutaq
Perseus 601X

Virtex-6 AMC with FMC site

PRODUCT SHEET



RoHS

FMC

µTCA

AdvancedMC™

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Nutaq **Perseus 601X**

- **Mid-size AMC for µTCA and AdvancedTCA platforms**
- **Choice of powerful LXT and SXT Virtex-6 FPGAs**
- **High-pin-count VITA 57.1 FMC expansion site for I/Os**
- **DDR3 SODIMM interface to upgrade system memory**
- **Supports multiple switch fabrics (PCIe, SRIO, XAUI, GigE)**
- **Comprehensive line of software development tools**

The Perseus 601X advanced mezzanine card (AMC) is designed around the powerful Virtex-6 FPGA, combining unsurpassed fabric flexibility and a colossal external memory, as well as benefiting from multiple high-pin-count, modular add-on FMC-based I/O cards.

The Perseus 601X is intended for high-performance, high-bandwidth, low-latency processing applications. The card also takes full advantage of the Virtex-6 FPGA's power, which, when combined with Nutaq's advanced software development tools, makes the Perseus 601X perfect for reducing size, complexity, risks and costs associated to leading-edge telecommunications, networking, industrial, defense and medical applications. On top this, the Perseus 601X's FMC expansion site offers almost endless I/O possibilities.

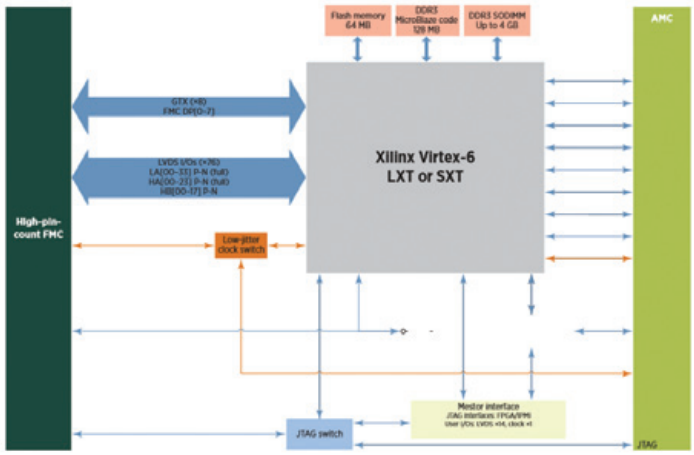
HARDWARE ARCHITECTURE

The Perseus 601X is designed around the latest Xilinx FPGA — the high-performance Virtex-6. The card can support the LXT and the SXT platform families, which both offer the flexibility and acceptable tradeoffs between high-performance logic and massive digital signal processing power.

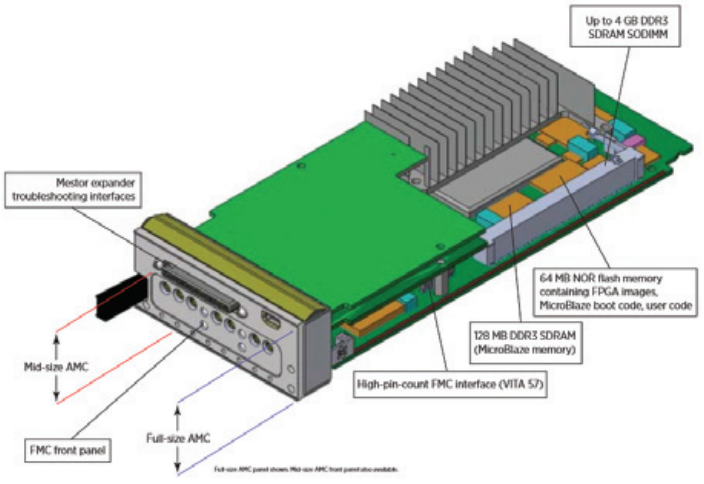
Features

- Support for AMC R2.0 and R1.0 through onboard clock switch
- Available GTX base clocks — 100 MHz, 125 MHz, 156.25 MHz (PCIe/GigE/XAUI/SRIO)
- Fabric clock — RX or TX (100 MHz PCIe, default)
- IPMI controller (based on the AVR version of the Pigeon Point AdvancedMC MMC)
- FPGA and IPMI JTAGs on the Mestor interface

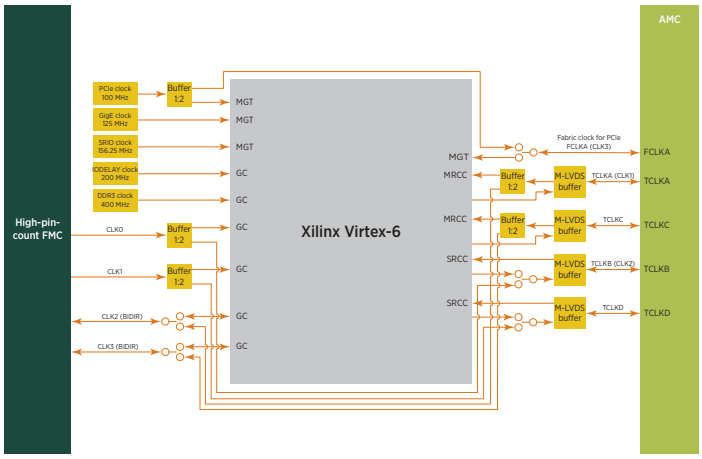
Perseus 601X functional block diagram

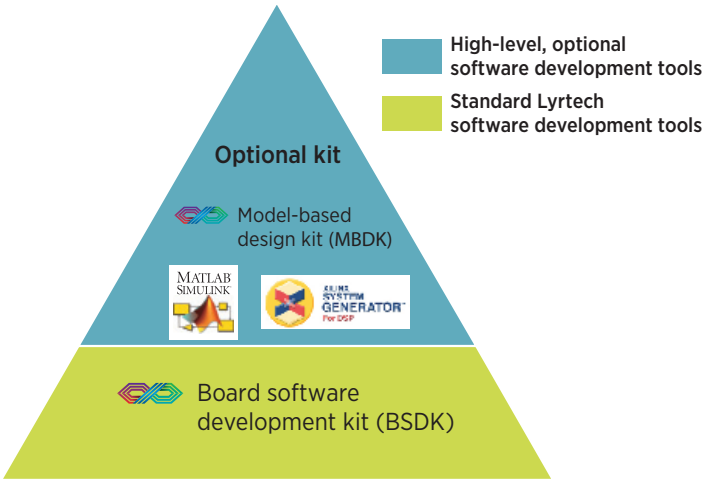


Perseus hardware architecture



Perseus 601X clock configuration diagram





DEBUGGING INTERFACES

The FPGA and IPMI JTAGs are available from the standard AMC backplane or from the onboard Mestor interface. Nutaq offers two optional Mestor debugging modes:

Mestor-to-FPGA JTAG adapter

Offers direct, onboard access to the FPGA's JTAG chain.

Mestor expander

Offers front-panel accesses to the FPGA and IPMI JTAGs, 14 user LVDS I/Os, one clock, and an FPGA UART interface (serial RX/TX—Mini-B USB). Note, however, that using the Mestor expander, transforms the Perseus 601X's form factor into a full-size AMC, thus the expander is supplied with a full-size face plate for the Perseus 601X.

PROCESSING POWER

The Virtex-6 family of FPGAs is the high-performance silicon foundation for targeted design platforms. Consuming 50% less power and costing 20% less than the previous generation of FPGAs, the Virtex-6 family is built with the right mix of programmability, integrated blocks for digital signal processing, memory and connectivity support — including high-speed transceiver capabilities — to satisfy the insatiable demand for higher bandwidth and higher performance.

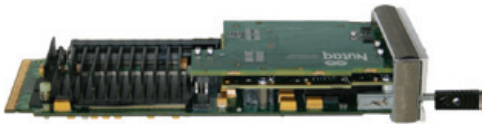
SOFTWARE DEVELOPMENT TOOLS

The Perseus 601X comes with a comprehensive set of integrated, multilayer software development tools that offer users a choice of environments — from a base-level hand-coded design environment to a high-level graphical model-based design environment.

Mestor adapter

Mestor expander

Persues 601X



Board Software Development Kit

Commonly referred to as the BSDK, this kit offers reconfigurable FPGA components and reference designs, along with the infrastructure to implement, simulate, synthesize, validate, and deploy complete applications on the card's Virtex-6 FPGA. This development kit takes care of the tiresome burden of reinventing interface drivers for the FPGA, freeing you to focus on unique, value-added development.

The kit includes a complete and fully tested set of Virtex-6 interfaces to all the Perseus 601X's peripherals:

- High-speed GTX transceivers

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- External memory controllers
- MicroBlaze instantiation and startup through a Linux kernel running Nutaq's central communication engine (CCE) server application
- External control through PCIe and GigE
- APIs and graphical interfaces for remote board management (such as FPGA application deployment, parameter control and data streaming)

The BSDK also offers:

- An array of reference designs for quick code implementation
- Applicative examples
- Streamlined debugging tools capable of recording/playback from external memory and more
- An unsurpassed integration to the model-based design workflow. Keep reading for details.

Model-Based Design Kit

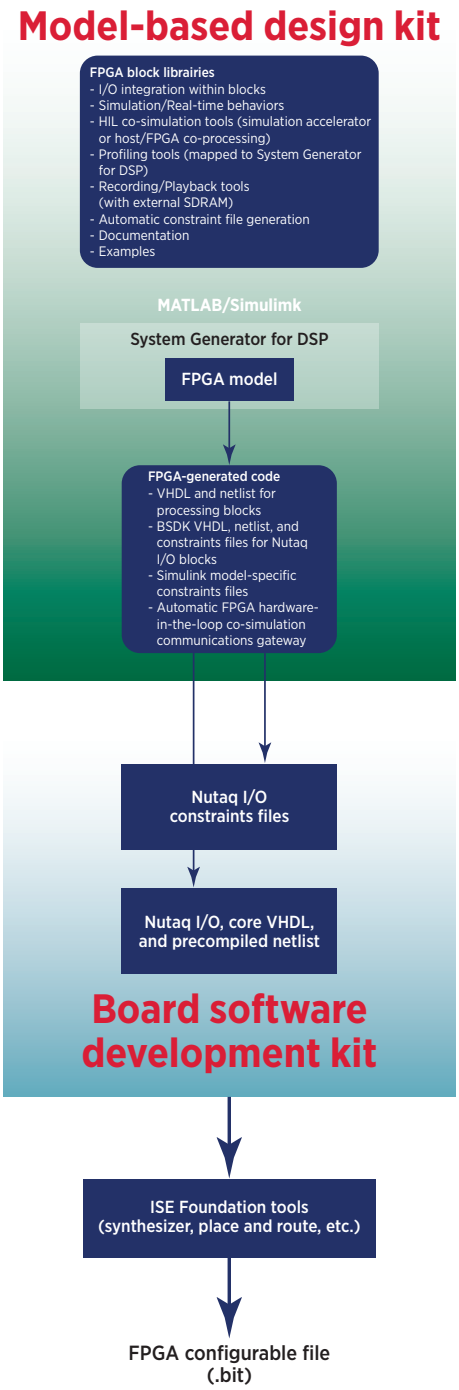
The optional Perseus 601X MBDK allows you to easily design high-performance digital signal processing systems within the card's FPGA with the MATLAB/Simulink design environment and extensive DSP IP libraries from Xilinx.

For even greater flexibility, System Generator for DSP supports MicroBlaze soft processor cores, which allows using high-level abstractions that can be automatically compiled into the FPGA without losing any performance over VHDL designs. Use it with ChipScope Pro to debug your applications.

These features, combined with the capabilities of the Virtex-6 FPGA, make it simple for designers to harness the parallel processing power of an FPGA.

THE PERSEUS MBDK EDGE

- Interface and integrate with the interface libraries supplied with the Perseus in no time flat.
- Benefit from all-integrated configuration, simulation, and code generation advantages of the Perseus' MBDK.
- Save precious development time using the debugging tools part of the MBDK, namely recording/playback tools and shared-memory GigE/PCIe HIL co-simulation tools.
- Configure the Perseus in a snap with its graphical configuration tools.
- Draw the maximum out of the Perseus' streaming interface between the FPGA and host computer running MATLAB (GigE/PCIe).
- Further your understanding of the Perseus with its extensive library of demonstrations and applicative examples.



Nutaq **Perseus 601X**

SPECIFICATIONS

FPGA

Xilinx Virtex-6 FPGA

- Perseus 6010: LX240T
- Perseus 6011: LX550T
- Perseus 6012: SX315T
- Perseus 6013: SX475T

Memory

- Up to 4 GB, 64-bit DDR3 SDRAM SODIMM
- 64 MB NOR flash memory (16 bits) — for FPGA images, MicroBlaze boot code and user code
- 128 MB DDR3 SRAM (8 bits) — for MicroBlaze FPGA applications

AMC connectivity

- Two GigE ports (ports 0–1)
- Two storage ports (ports 2–3)
- Flexible fat pipes (ports 4–11) PCIe/SRIO/GigE/XAUI
- User LVDS I/Os (ports 12–15)
- RTM GTXs (ports 17–20)
- TCLK A/B/C/D support for AMC R2.0/R1.0 through onboard clock switch
- Fabric clock — RX or TX (100 MHz PCIe, default)

Front panel

- Mid-size AMC
  - Board mounted LEDs
  - FMC slot
- Full-size AMC
  - Mestor expander slot
  - Board mounted LEDs
  - FMC slot

I/O expansion capabilities

- High-pin-count VITA 57.1 FMC site
  - 8× GTX transceivers FMC DP[0–7]
  - 76× LVDS I/O [LA00-33/HA00-23/HB00-17]
  - 4× clock (2× FMC to FPGA and 2× bidirectional FMC to/from FPGA)
- Mestor interface (debugging ports/control I/Os)
  - FPGA and IPMI JTAGs
  - LVDS user I/Os (×14), clock (×1)
  - FPGA UART interface (serial RX/TX) [front panel mini-B USB interface on Mestor expander]

Mechanical

- Mid-size AMC
- Full-size AMC — with optional Mestor expander
- AMC B+ edge connector

IPMI controller

- Voltage monitor
- Geographical address monitor
- Temperatures monitors
- Power/Reset controller
- UART

Standards compliance

- AdvancedTCA base 3.0 (PICMG 3.0/3.1/3.4/3.5)
- AdvancedMC R2.0 (PICMG AMC.0/AMC.1/AMC.2/AMC.3/AMC.4)
- Support for AdvancedMC R1.0 also available
- QTCA R1.0
- VITA 57.1 FMC HPC (supports the rugged and commercial form factors)
- Hot swap
- PMI

Testing and development interfaces

- Mestor interface — FPGA JTAG, IPMI JTAG, mini-B USB serial port, GPIOs)
- Test points
- Jumpers
- Software switches
- USB
- LEDs

Electrical

- AMC 12 V main source, 3.3 V IPMI

Power consumption

- Total: less than 40 W (with LX240T)
- Bias: 9 W (at startup, FPGA not loaded)
- CCE default application loaded, over Linux MicroBlaze: 12 W (CCE loaded, on stand-by, FPGA I/Os mapped)

Environmental

Contact Nutaq for details about this specification.

FMC options

ADAC250

- Two, 250 MSPS, 14-bit ADCs
- Two, 1 GSPS, 16-bit DACs

2×10GE SFP+

•Two-port, 10 GE SFP+ FMC

QSFP/SFP+

- One straight QSFP(+) port
- Two straight SFP(+) port

MI125

16x/32x, 125 MSPS, 14-bit ADCs

ADC550

Two, 550 MSPS, 12-bit ADCs

ADC5000

- Four, 1.25 GSPS, 10-bit ADCs;
- or two, 2.5 GSPS, 10-bit ADCs;
- or one, 5 GSPS, 10-bit ADC

Radio420S

- One RF transceiver (300 MHz–3 GHz)
- Programmable bandwidth (1.5–28 MHz)

Radio420M

- Two RF transceiver (300 MHz–3 GHz)
- Programmable bandwidth (1.5–28 MHz)
- Forces using the full-size AMC form factor

Nutaq products are constantly being improved; therefore, Nutaq reserves the right to modify the information herein at any time and without notice. The FMC logo is a trademark of VITA.

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