Nutaq
μSDR420

FPGA-based, MIMO-Enabled, multimode, tunable RF SDR solutions

PRODUCT SHEET

Nutaq® Defense

QUEBEC | MONTREAL | NEW YORK | nutaq.com

Nutaq **µSDR420**

- **SISO, dual-band and N x N MIMO RF transceivers**
- **Wide frequency range — 0.3–3.0 GHz**
- **Selectable bandwidth — 1.5–28.0 MHz**
- **Combines Virtex-6 with Nutaq's Linux embedded OS framework**
- **Supports remote GigE access from Windows and Linux**
- **Supports embedded applications trough Linux processor blade option**
- **Develop applications more quickly with model-based design**

The µSDR420 is a customizable, embedded SDR solution that incorporates tremendous FPGA logic and memory, as well as a powerful multimode SDR single/dual-channel RF transceiver module that can be stacked together to form a complete n channels turnkey solution from baseband processing to the air interface. The µSDR420 is capable of uplinking and downlinking data streams to a remote computer running on Linux or Windows through high-speed GigE interfaces. Embedded baseband processing is enabled trough the addition of a µTCA processor blade (Linux only). In such configuration, up to an 8x PCIe link can be used to stream data on the backplane.

µSDR420s greatly reduce your time to market, bringing the performance that you need to a wide range of applications such as multimode SDR, advanced telecommunications (MIMO systems, cognitive radios, LTE, WiMAX, white space, Wi-Fi, GSM, WCDMA), and signal intelligence (SIGINT).

MULTICHANNEL EXPANSION

Based on the µTCA architecture, the µSDR420 has limitless channel expansion capability and offer the number of AMC slots necessary to any specific application. The µSDR420 also benefit from ultra-high bandwidth crosspoint links between FPGA elements (through the µTCA backplane), making it possible to add DSP algorithms that can be simultaneously applied to all system channels — useful in such applications as MIMO, or beamformers.

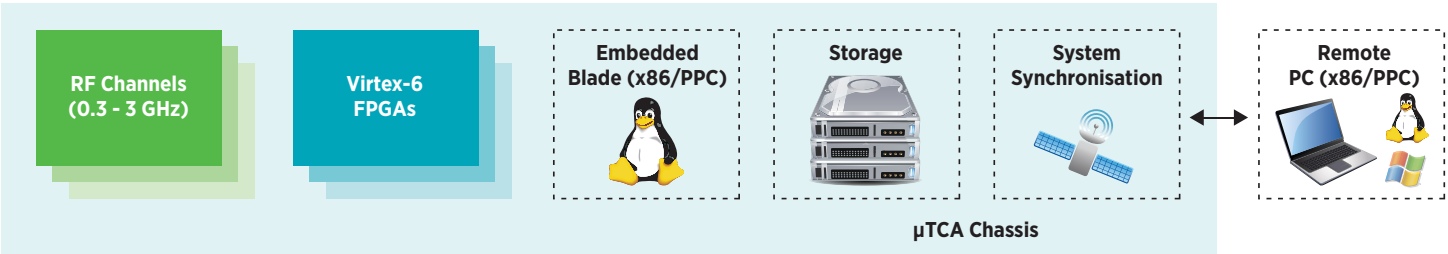
FULLY INTEGRATED SOLUTION

The µSDR420 integrates a complete array of tools and capabilities for added efficiency and ease of use:

- Available FPGA for intensive processing, down-converter, up converter space-time coding, waveforms PHY layer (such as OFDM)
- Complete Nutaq FPGA framework, including embedded Linux MicroBlaze Ethernet/PCIe server
- Real-time GigE data exchanges between a host device CPU (Linux or Windows) and PCIe data streaming tools (Linux only)
- Multichannel recording and playback tools (DAQ applications)
- Local (embedded AMC processor blade) and remote access
- Real-time and hardware-in-the-loop cosimulation with the FPGA
- Seamless integration to the MATLAB/Simulink model-based design flow
- Stand-alone operation, running directly from the flash/HDD memory
- Graphical control applications

FLEX OFDM REFERENCE DESIGN

A complete OFDM QAM4/QAM16 FPGA PHY layer is available for Model-based design Simulink users. The Framework shows real-time wireless video transmission between two transceivers through SISO or MIMO 2x2 RF interfaces. Constellation and other parameters directly accessible from the Simulink environment. Simulink models provided as source files.



FPGA SECTION

The Perseus making up the FPGA section of the µSDR420, is designed around the high-performance Virtex-6, which offers the flexibility and tradeoffs between high-performance logic and massive digital signal processing power.

FEATURES

- Supports LX240T, LX550T, SX315T, and SX475T FPGA devices
- Supports PCIe (1×, 4× and 8×)
- Fabric clock — RX or TX (default 100 MHz PCIe)
- IPMI controller (based on the AVR version of the Pigeon Point AdvancedMC MMC)
- FPGA and IPMI JTAGs on the Mestor interface
- Includes a complete framework of Virtex-6 interfaces to all the FPGA section's peripherals:
- High-speed GTX transceivers
- External memory controllers
- MicroBlaze instantiation and startup through a Linux kernel running Nutaq's central communication engine (CCE) server application
- External control through PCIe and GigE
- APIs and graphical interfaces for remote or local management (such as FPGA application deployment, parameter control and data streaming)

EMBEDDED PROCESSOR SECTION

The µSDR420 can be equipped with cutting-edge embedded processor options and a complete Linux framework APIs and application examples.

AMC GPP module options

- Intel Next Gen CoreTM i(Gladden), 4Core 2 GHz 16GB DDR-III
- CPU: AMC, Full-Size P2020 1.2 GHz processor

Note: SATA and solid-state HDDs are available as options.

RADIO SECTION

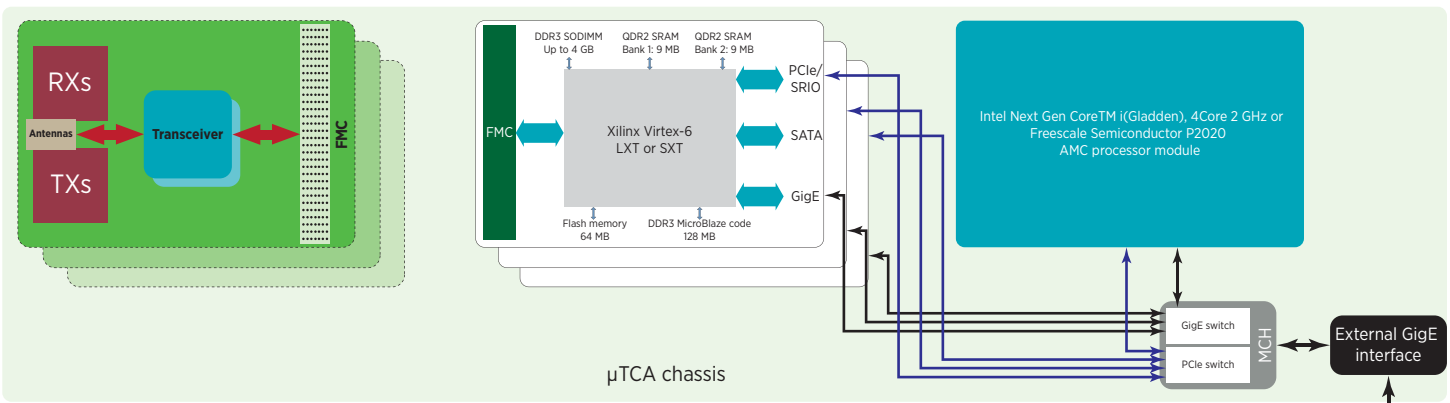
The radio section (based on Radio420x) is equipped with two state-of-the-art multimode, multiband RF transceivers that support operation anywhere between 0.3 GHz and 3 GHz, TDD or FDD. Its selectable bandwidth (1.5 MHz to 28 MHz) makes it suitable for a large number of narrowband and broadband applications with excellent channel selectivity.

SPECIFICATIONS

FPGA

Xilinx Virtex-6 FPGA:

- Perseus 6010: LX240T
- Perseus 6011: LX550T
- Perseus 6012: SX315T
- Perseus 6013: SX475T



Example—Radio420S FMC
(Others available)

- Frequency range — 0.3–3 GHz
- Selectable bandwidth — 1.5–28 MHz
- Multiple reference configurations and expansion modes
- Individually shielded RX and TX analog paths

Perseus 601X

- Choice of LXT and SXT Virtex-6 FPGAs
- DDR3 SODIMM interface to upgrade system memory
- 18 MB QDR2 SRAM (18 bits)
- Supports multiple switch fabrics (PCIe, SRIO, XAUI, GigE)

FPGA memory

- Up to 4 GB, 64-bit DDR3 SDRAM SODIMM
- 18 MB QDR2 SRAM (18 bits) — two banks of 9 MB
- 64 MB NOR flash memory (16 bits) — for FPGA images, MicroBlaze boot code and user code
- 128 MB DDR3 SRAM (8 bits) — for MicroBlaze FPGA applications

Radio

- 0.3 – 3.0 GHz
- Dual SISO/2×2 MIMO per FMC card.
- 1.5 MHz to 28.0 MHz bandwith

Embedded GPP (optional)

Intel option

- Intel Next Gen CoreTM i(Gladden), 4Core 2 GHz 16GB DDR-III
  - CPU: AMC, Full-Size Intel Next Generation CoreTM i (Gladden), 4 Core, 2 GHz processor
  - Single-width, full-size
  - 8MB LLC
  - 16 GB DDR-III ECC memory
  - 16 GB Flash
  - PCIe (Port 4-7)
  - Front Panel GigE & USB ports

or

- CPU: AMC, Full-Size P2020 1.2 GHz processor
  - Single-width, full-size
  - 4 GB DDR-III ECC memory

- 32Mbytes of NOR Flash
- 256 Mbytes of NAND Flash
- PCIe (Port 4-7)
- Front Panel GigE

Electrical

External universal 110/220 V AC (–48 V DC standard telecommunications supply also available. Contact Nutaq for details.)

Standards compliance

- AdvancedTCA base 3.0 (PICMG 3.0/3.1/3.4/3.5)
- AdvancedMC R2.0 (PICMG AMC.0/AMC.1/AMC.2/AMC.3/AMC.4)
- Support for AdvancedMC R1.0 also available
- µTCA R1.0
- VITA 57.1 FMC HPC
- Hot swap
- IPMI

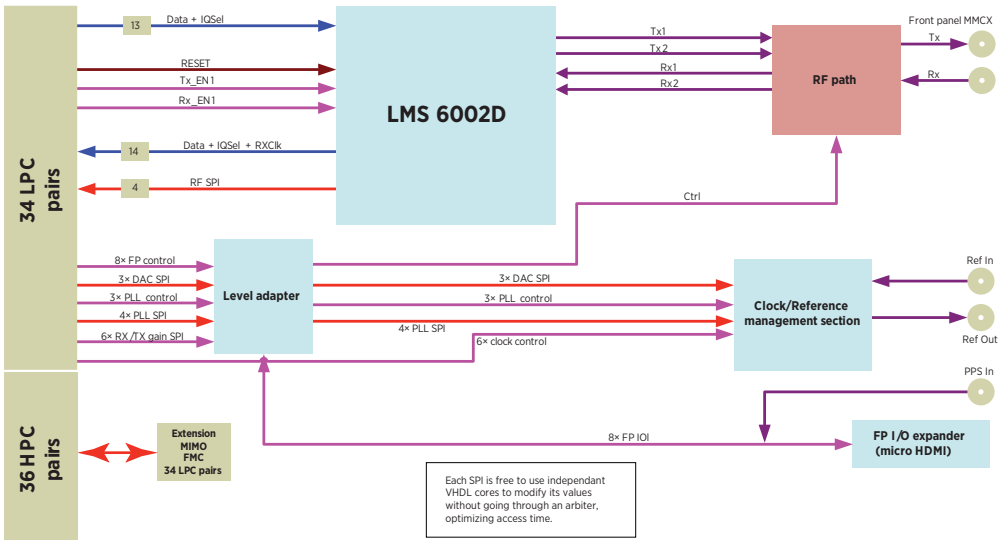
Mechanical

- Depends on configuration

Power consumption

- Depends on the configuration

Radio section



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ORDERING OPTIONS

µSDR420-XYZ-ABC-DEF-GHJ-K

- **XYZ** = # of RF transceivers and FPGA processors

S01 = 1x SISO Transceiver	1x FPGA (fit Mid-size AMC's slot)
M21 = 2x2 MIMO or 2x independent Transceivers	1x FPGA (fit Full-size AMC's slot)
M41 = 4x4 MIMO or 4x independent Transceivers	1x FPGA (fit Double-width, Full-size AMC's slot)*
M42 = 4x4 MIMO or 4x independent Transceivers	2x FPGA (fit Full-size AMC's slot)
M82 = 8x8 MIMO or 8x independent Transceivers	2x FPGA (fit Double-width, Full-size AMC's slot)*
M84 = 8x8 MIMO or 8x independent Transceivers	4x FPGA (fit Full-size AMC's slot)

- **A** = FPGA Type/Size
  - 0 = LX240T Virtex-6 FPGAs
  - 1 = LX550T Virtex-6 FPGAs
  - 2 = SX315T Virtex-6 FPGAs
  - 3 = SX475T Virtex-6 FPGAs
- **B** = FPGA Speed Grade
  - 0 = -1
  - 1 = -2
  - 2 = -3 (only with LX240T or SX315T)
- **C** = DDR3 FPGA SODIMM Size
  - 0 = 1 GB
  - 1 = 4 GB
- **D** = Synchronization options
  - 0 = All transceivers on-board clocks or External clock provided externally provided by end user
  - 1 = Include uSync board. All transceivers synchronized by a common reference. GPS disciplined clocks included.
- **E** = Baseband processor options (GPP baseband-network processor)
  - 0 = No GPP, all FPGA boards can be accessed trough remote GigE PC. (PCIe backplane streaming not available in such configuration)
  - 1 = Intel Next Gen CoreTM i(Gladden), 4Core 2 GHz 16GB DDR-III (PCIe backplane streaming enabled)
  - 2 = P2020 1.2 GHz 4GB DDR-III (PCIe backplane streaming enabled)
- **F** = Storage options
  - 0 = No HDD. If GPP included (option E), Linux OS installed to on-board flash.
  - 1 = SATA-II Drive Module 500 GB
  - 2 = SATA-II Drive Module 1 TB
  - 3 = SSD SATA-II Drive Module 600 GB (Higher performance & reliability)
  - 4 = SSD SATA-II Drive Module 1.2 TB (Higher performance & reliability)
- **G** = Operating Temperature
  - 0 = Commercial Temp
  - 1 = Industrial Temp*
- **H** = Development Software
  - 0 = BSDK. Include Host development and FPGA development Framework.
  - 1 = MBDK. Include BSDK + Model-based FPGA development within Simulink and Host co-simulation Simulink tools.
- **J** = Debugging
  - 0 = No debugging tools (Not recommended for application development phase)
  - 1 = Flex Mestor expansion kit to all FPGA boards.
  - 2 = Mestor expansion kit to all FPGA boards (Includes Mestor Breakout Box).**
- **K** = Flex OFDM
  - 0 = Not included
  - 1 = Includes Simulink Flex OFDM Reference design model.***

* Contact info@nutaq.com for availability

** Does not fit to all FPGA board configurations. Cannot fit on double-stacked FMCs.

*** Requires MBDK software (option H = 1)

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