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Prototyping a MIMO W-CDMA system using a system-level approach

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Abstrad—This paper describes the development and proto-typing of a MIMO (Multiple-Input Multiple Output) wireless link designed to operate under the WCDMA third generation cellular standard. The said development is performed in an integrated, system-level fashion on a DSP/FPGA development platform, the Nutaq SignalMaster.The first part of the paper will succintly describe the evolution and the main features of the WCDMA standard. Likewise, the second part reviews the basic concepts of space-time processing and MIMO communications. The third part details the system-level design flow and prototyp-ing approach exploiting the strong linkage between Simulink and the SignalMaster platform. Finally, preliminary implementation results and comparisons with other design and prototyping tools and approaches are provided.

I. INTRODUCTION

Wireless cellular telephony nowadays is characterized by a multitude of standards including the still-in-use venerable first-generation AMPS (analog cellular in the 800 MHz range) standard, the globally successful second-generation (2G) GSM standard (operating in 3 different bands in different regions of the globe: 900, 1800 and 1900 MHz), other 2G standards such as IS-95, IS-136, PDC, and emerging third generation (3G) standards such as EDGE (Enhanced Data rates for GSM Evo-lution), WCDMA (Wideband Code-Division Multiple Access) and cdma2000.

The evolution of wireless cellular is naturally evolving towards broadband wireless access characterized by high data rates, a multiservice, packet-based infrastructure (thus break-ing free from the classical switch-based telephone paradigm). 3G systems (and most notably WCDMA) should in principle offer full-duplex 2 Mbps data rates. As they are slowly beingd eployed, however, it seems that maximum effective rates are in fact 384 kbps downstream and 64 kbps upstream. This suggests that true broadband access in the current cellular evolution path will have to wait for the advent of 4G.

Wireless LAN technology, however, has been a huge com-mercial success under the auspices of the 802.11a/b/g (WiFi) standards which present the advantage of low-cost availability of both service and hardware almost anywhere on Earth. The so-called WiFi technology readily offers nominal data rates of 11 and 54 Mbps

(although in practice, throughput is typically limited to approximately 32 Mbps). Is WiFi the broadband access system of the future? Not quite, despite the huge interest it generates in cellular service providers. Indeed, while it does offer the high data rates, 802.11 as it stands today offers very limited support for mobility, both in terms of roaming support (handover) and dealing with hostile Doppler effects generated by high-speed mobility. It is well-known that the relatively low data rates in cellular are mainly due to Doppler-induced fast variations in the channels. Furthermore, 802.11 has a very limited range because of the transmit power limitations imposed in the unlicensed bands it exploits. Finally, operation in unlicensed bands does entail unknown interference conditions as well as increased spectrum crowding due to WiFi's own success. However, the continuing evolution of 802.11 and similar technologies suggests a convergence with cellular, as range is increased and higher levels of support for mobility are incorporated.

This multitude of coexisting standards and the attractiveness of offering in many devices both the high bandwidth of WiFi and the mobility / network integration of cellular creates a particularly challenging context for wireless system designers. Time-to-market windows are also very short, thus creating a need for highly-streamlined, efficient design flows.

The need to be compliant with several standards drives the continuing development of reconfigurable radio technol-ogy. Historically, this has been termed software-defined radio (S DR) technology since it was originally conceived in the form of a software-only implementation of the radio transceiver running on a DSP platform. However, it has become obvious that even the considerable processing power of DSPs was not enough in many circumstances and that FPGAs (Field Programmable Gate Arrays) were called for.

Be that as it may, SDR is recognized as a key enabling technology for future wireless systems. In fact, a multitude of european projects (CAST, PASTORA, TRUST, STINGRAY) are evolving the SDR concept in various directions. In the US, SDR research is manly driven by the Dept. of Defense (DoD). In a large effort to produce widely capable and adaptable systems, SDR efforts are channelled through the Software Communication Architecture (SCA) under the umbrella of the Joint Tactical R adio System (JTRS) program [1]. A number of acquisition programs are currently requesting SCA compliance (e.g. DMR, CAMP). Also, very advanced uses of SDR con-cepts are now proposed, such as very-high density and multi-waveform systems (such as in the AMF cluster) and “wireless and available bandwidth sensing” radios, dubbed as “cognitive radios”.

II. THE WCDMA STANDARD

Out of a plethora of options, WCDMA technology has emerged as the most widely-adopted air interface for 3G cellular telephony in the standardisation process [3, p.1]. Its specification was drafted to support multiservice, packet-based network integration with multimedia applications in mind. WCDMA aims to provide bit rates up to 2 Mbps, vari-able bit rates (bandwidth-on-demand), all with high spectrum efficiency and the coexistence of FDD (Frequency-Division Duplexing) and TDD (Time-Division Duplexing) within the standard. It is further characterized by the a set of quality-of- service (QoS) classes and the multiplexing of services with different quality requirements on a single connection. It utilizes a wide carrier spacing of 5 MHz with fast power control on both uplink and downlink. Complying with a pure version of the CDMA paradigm, the frequency reuse factor is 1 and frequency diversity is obtained through the use of Rake receivers.

It is noteworthy that simple downlink transmit diversity using Alamouti’s space-time code [4] is part of the standard, and that a “door is left open” for proprietary, more complex space-time processing and MIMO schemes. This is in contrast with 2G where application of space-time techniques are either impossible or very difficult to implement since no provision for them is provided by the standards.

WCDMA is a direct-sequence spread spectrum system with both spreading and scrambling. When either the base station or the terminal transmits, the data is first multiplied continuously by the channelization cod e, bringing the signal from bit rate to chip rate (where chip rate refers to the smaller symbol period in the code).

Then, a second mixer multiplies the chip rate signal by the scrambling code. Since the latter is also at chip rate, no further spreading occurs at this step.

In order to support multirate operation, spreading (channel-ization) codes are based on the Orthogonal Variable Spread-ing Factor scheme (OVSF) [5]. It is thus possible to vary the spreading factor while maintaining orthogonality between codes. Channelization codes are used to distinguish multiple signals coming from the same source, e.g. the base station in a given sector. Thus, each source can select codes independently.

Scrambling codes are Gold / Kasami sequences and are used to differentiate sources from one another. Thus, these codes are subject to a global allocation strategy, but the latter is simplified because the multirate aspects are entirely handled by the channelization codes.

A single transmission normally includes two channels, the DPDCH (data) channel and the DPCCH (control) channel. These are separable at the receiver because they are spread by different channelization codes. The two spreaded signals are then added up in quadrature before complex scrambling and upconversion.

Mathematically, a transmitted WCDMA signal is given by

$$u(t) = \sum_{k=0}^{K-1} a_k \sum_{n=0}^{N-1} p_k(n) f(t - nT - kNT), \qquad (1)$$

where ak is the complex transmitted symbol, pk is the com-plex code resulting from the cascade of the spreading and scrambling codes, N is the spreading factor, f(t) is the pulse shaping filter (root raised-cosine with roll-off factor 0.22) and T is the chip duration.

The received signal y(t) at the other end of the wireless link is given by

$$y(t) = \sum_{j=0}^{J-1} c_j u(t - \tau_j) + g(t), \qquad (2)$$

where the mobile channel is modeled as a filter with complex taps ci and delays ½j, where { j = 0, 1, ··· , J - 1 } for a total of J different paths, and g(t) is the additive white Gaussian noise (AWGN) process with a single-sided power spectral density (PSD) of N0.

The first step in the reception chain consists in having the received signal pass through a matched filter. The said filter is matched to the transmitted pulse shape and it is in fact a root raised-cosine filter. A path searcher then estimates the delay ½j of each significant path in the channel impulse response. Then the received signal is delayed by the amount estimated by the searcher and multiplied by the conjugate of the scrambling/spreading code combination used at the transmitter. The descrambled and despread data are then summed over one symbol period:

$$x_k(\hat{\tau}_j) = \frac{1}{N}\sum_{m=0}^{N-1} p_k^*(n) r(t + mT - kNT), \qquad (3)$$

for all delays ˆ ½j that correspond to a strong path (where ˆ ½j is the estimate of the real path delay ½j). These estimates are then weighted and summed by the RAKE combiner so that their energy add up coherently:

$$\hat{a}_k = \det\left\{\sum_{j=0}^{\hat{J}-1} \hat{c}_j^* x_k(\hat{\tau}_j)\right\}, \qquad (4)$$

where cj is the complex channel gain estimate at delay ˆ ½j , ˆ J is the estimated number of strong paths, det(·) is a simple decision device, and ˆ ak is the estimated bit / symbol obtained at the output of the RAKE receiver.

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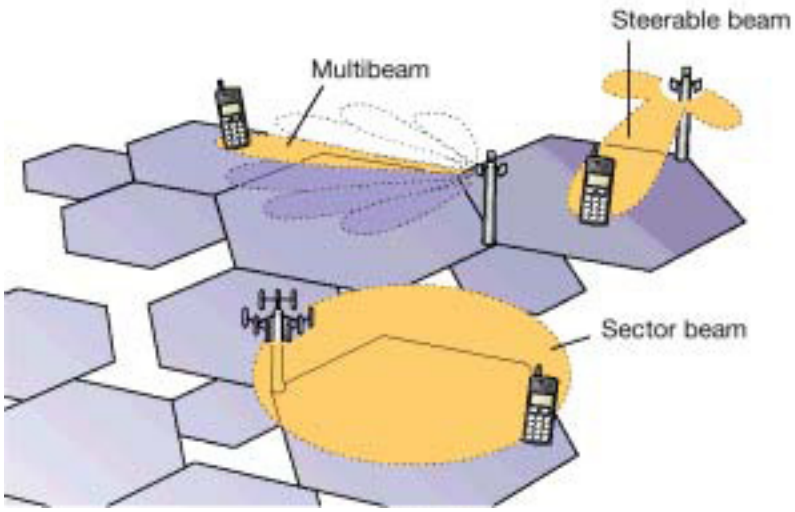
IV. RAPID PROTOTYPING DESIGN FLOW

It is a documented fact that current wireless systems and products are characterized by very short production cycles. This puts considerable pressure on an increasingly short design cycle. In fact, actual physical prototyping is nowadays often skipped altogether with a product moving directly from computer simulation to production. However, even this drastic practice does not streamline the design cycle enough. It has been suggested in [7] that a unified design flow, from the initial reference model to the final implementation, is desirable. The proposed flow was dubbed the Five-Ones Approach: one team, one environment, one code, one documentation and one code revision tool.



a)

b)

Fig. 1. Adaptive antenna arrays and beamforming: (a) various forms of beamforming in cellular systems; (b) Japan's 4G high-atmosphere airborne base station platforms using adaptive antenna arrays.

To address the challenge of designing complex wireless systems, the developers need tools that complement their expertise and address all the difficult interoperability and high performance issues at the simulation and verification level prior to and / or during implementation and testing phases. Design verification models can be expanded and synthesized for specific target hardware, using heterogeneous simulation and co-verification approaches.

The Nutaq SignalMaster platform is a powerful pro-totyping tool because it provides a tightly-coupled DSP/FPGA pair and close integration with Matlab / Simulink and Xilinx's System Generator. It is an ideal platform to support a unified design flow such as the Five Ones Approach. Indeed, from the initial reference model in Simulink, it is possible to perform PC-based simulation, Hardware-in-the-loop simulation (with the SignalMaster's DSP and / or FPGA accelerating the simulation), DSP / FPGA design partitioning, synthesis, optimization, and actual real-time prototyping with the SignalMaster interfaced to external hardware if necessary. Throughout these steps, Simulink remains the unifying design environment.

In the wireless design process, increasingly complex chan-nel models must be used in simulations to realistically assess system performance. These models must take into account the statistical behavior of various phenomena: shadowing (long-term fading), multipath (short-term fading), Doppler spread, angle spread (related to the topology of the scattering region) and in MIMO, correlations between the signal envelopes received / transmitted from different antennas. Simple models can be used to model multipath fading (Rayleigh, Rice, Nak-agami), more complex models (GBSBEM, GBSBM, GWCM [8]) are needed for MIMO and for modeling the statistical behavior of the directions-of-arrival and Doppler spectra.

A design and simulation environment such as Simulink allows the modeling of both the channels and the systems themselves. For example, Figure 2 shows a “classical” simu-lation model where an entire FDD WCDMA link (including the channel) is simulated. In this model, one can find a mix of simulation primitives for DSP functions and C-code functions (applications previously developed independently). From these well-known classical simulation capabilities, the possibility of generating code for / synthesizing any or all of the components in the model can extend the simulation activity towards target implementation in an approach often referred to as rapid prototyping. Obviously, the implementation code thus generated is not optimal but the considerably shortened time to a working implementation model is of interest.

In fact, this so-called system -level development approach, is rich in implementation and testing capabilities. For example, it is possible to target intermediate or final hardware in such a way as to allow testing of target (implementation) code from within the simulation tool. Thus, previously implemented HDL code can be integrated in the simulation process in the form of a Simulink block. When using a hybrid DSP / FPGA architecture such as the SignalMaster platform, the model can be broken down in components for the DSP, the FPGA and the host [9].
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V. IMPLEMENTATION RESULTS

An ongoing project at the Laboratoire de Radiocommunica-tion et de Traitement du Signal (LRTS) at Laval University and the R2D2 research group at the École Nationale Supérieure de Sciences Appliquées et de Technologie (ENSSAT) con-cerns the efficient

implementation of novel MIMO algorithms adapted to the WCDMA context. The SignalMaster design flow is currently being investigated through the implementa-tion of a simple 2 × 2 MIMO WCDMA link. Figure 3 shows the block diagram of the 2-antenna transmitter. The 2 antennas can transmit independent bitstreams, each one being spread by a different channelization code. In order to stay within the parameters of the standard as much as possible, the same DPCCH information is transmitted on both antennas. Finally both antennas belong to the same source and therefore used the same scrambling code.

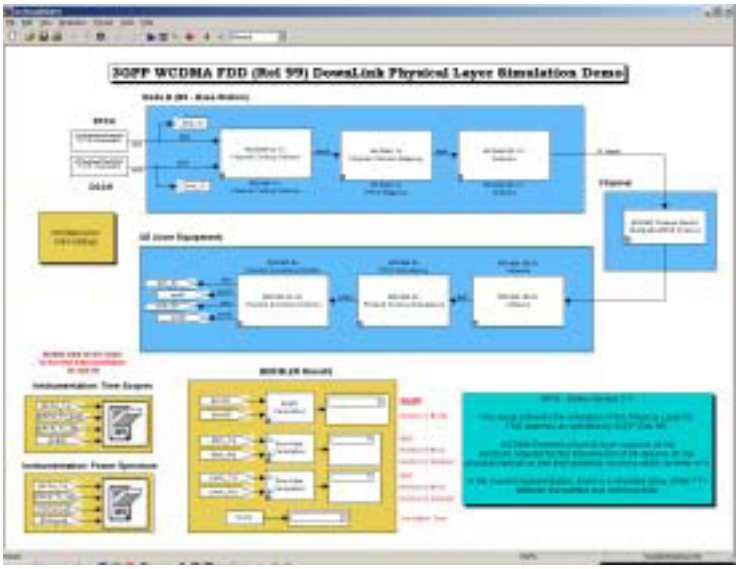

Fig. 2. Typical Simulink model for a WCDMA system

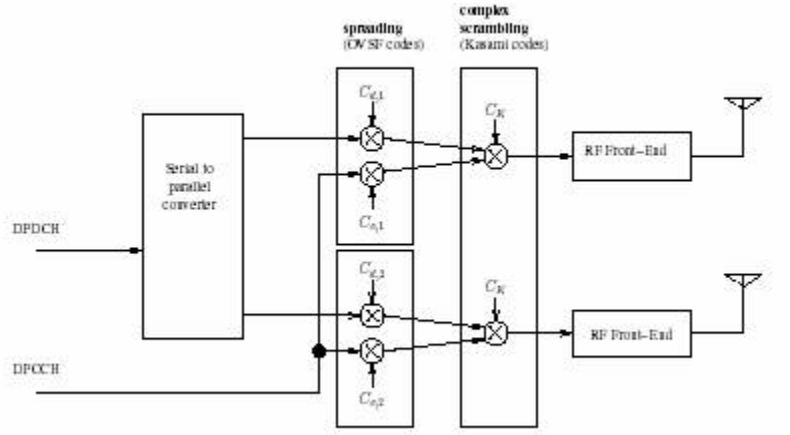

Fig. 3. Block diagram of MIMO WCDMA transmitter

Figure 4 shows the 2-antenna receiver structure. The stan-dard UMTS matched filtering (root raised cosine or RRCos) is applied. The incoming streams are oversampled at four times the chip frequency. The filtered signal is fed to a searcher block which performs the finger (path) search in the wideband impulse response. A description of this block is beyond the scope of this paper since it is significantly complex. It transmits the position of each finger to the RAKE blocks. There are four fingers per block, so that ideally, the four strongest paths in the impulse response are exploited. The RAKE block performs channel estimation, despreading and compensation of channel effects (e.g. cophasing). The sampled outputs of the RAKE filters as well as the channel coefficients are sent to a MIMO decoder which performs self-interference cancellation.

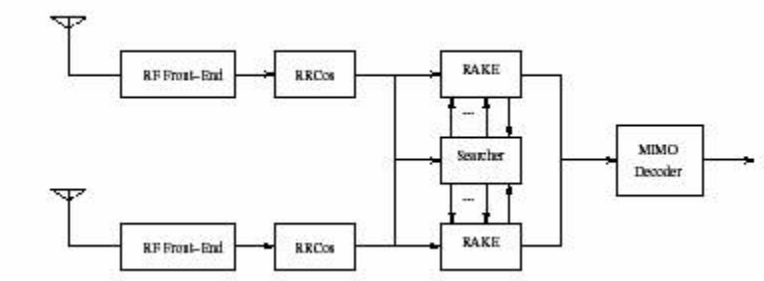

Fig. 4. Block diagram of MIMO WCDMA receiver

Implementation in a Xilinx Virtex-2000E FPGA shows that the RRCos filter (64 taps) requires 3 percent of the LUTs (look-up tables) while one complete finger requires 7 percent. They operate respectively at 49.1 MHz and 51.7 MHz. At this point in time, the entire reference model is functional in Matlab but only a few blocks have been implemented for the FPGA. The targeted implementation model is to have time-critical and complex functions implemented in the FPGA. The targeted implementati on model is to have time-critical and complex functions implemented in the FPGA, with state machines and other less speed-hungry components in the DSP. This will mirror as much as possible an actual product implementation, perhaps with FPGA and DSP on a custom single ASIC (with some FPGA blocks in the prototype actually corresponding to dedicated blocks, with the ASIC retaining a portion of FPGA fabric for flexibility).

An RF-prototyping platform is currently being constructed at Laval consisting of 3 stations with 4 antennas each and RF front-ends supporting unlicensed bands at 2.4 and 5.15 GHz. The acquisition and processing hardware is fully generic, supporting the SDR paradigm, and is completely comprised of SignalMaster hardware, thus providing an integrated, unified platform tightly integrated with the development software.

An example of such a prototyping platform, complete with RF front ends, is given in Figure 5. This system is equipped with 8 antennas and is based on Nutaq products. The SM-VHS-ADC and SM-HS-DAC are cPCI compliant cards which can form an 8-channel array-antenna high-speed data acquisition system for real-time processing applications. The SM-VHS-AD C's and SM-HS-DA C's pre-processing Virtex-II combined with the single or quad C6xx-based SignalMaster allows truly transparent 10/65/80/105 Msps / channel rate processing with Virtex-II FPGA's.

VI. CONCLUSION

This paper presented an approach for using high-level tools in an integrated design flow to rapidly design and prototype state-of-the-art wireless applications. As a case study, highlights and preliminary imlementation results were provided from an ongoing design project at Laval university involving the efficient implementation of MIMO algorithms for WCDMA. Depending on the application, it is believed that this type of system-level approach will become more and more relevant in coming years, considering the evolution of methodologies, programmable logic parts and the growing importance of SDR / reconfigurable radios.

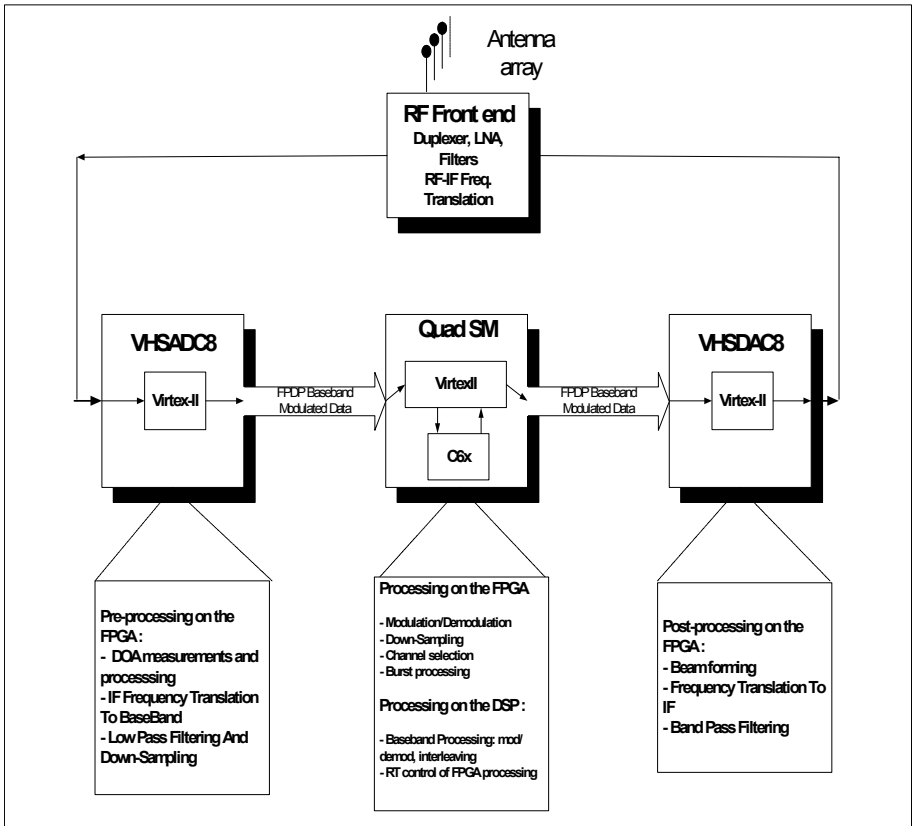

Fig. 5. Antenna array prototyping platform

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