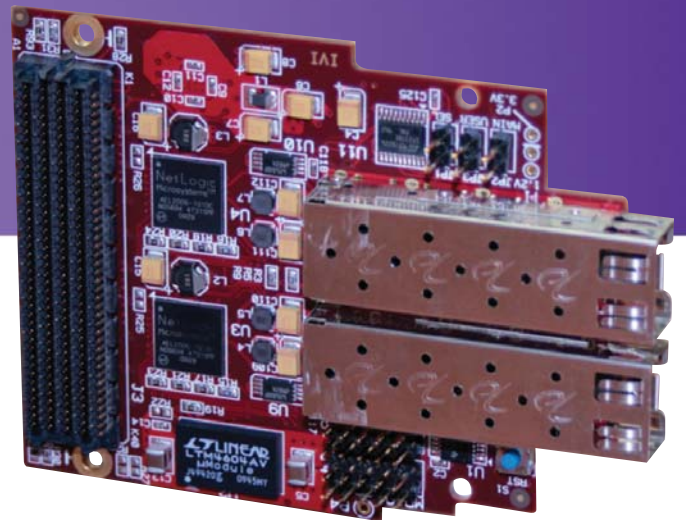


Nutaq 2x10GE SFP+

Two-port, 10 GE SFP+ FMC module
PRODUCT SHEET



Nutaq 2x10GE SFP+

- Versatile and industry-standard VITA 57.1 FMC module
- Two, front panel SFP+ ports

The 2x10GE SFP+ FPGA mezzanine card (FMC) is designed around the NetLogic Microsystems AEL2005 PHY, which interfaces to the FMC's I/Os with the XAUI protocol and creates SFP+ 10 Gbps interfaces using four, 3.125 Gbps FPGA transceivers. The AEL2005 is a physical layer transceiver with an integrated electronic dispersion compensation (EDC) engine that complies with the IEEE802.3aq specifications.

With its multiple clocking capabilities, the 2x10GE SFP+ can be used in limiting linear or twinaxial cabling (twinax) modes to answer the high data throughput needs of advanced Ethernet telecommunications applications. Further, the 2x10GE SFP+ complies to the VITA 57.1 standard, widely used by the digital signal processing industry, making it easier for developers to integrate FPGAs to their embedded system designs. The 2x10GE SFP+ is ready for use with Nutaq RD's μ TCA Perseus AMCs, but it can as easily be used on other AMCs.

The front panel SFP+ ports extend slightly outward from the front panel to comply with the mechanical specifications for FMCs.

Hardware architecture

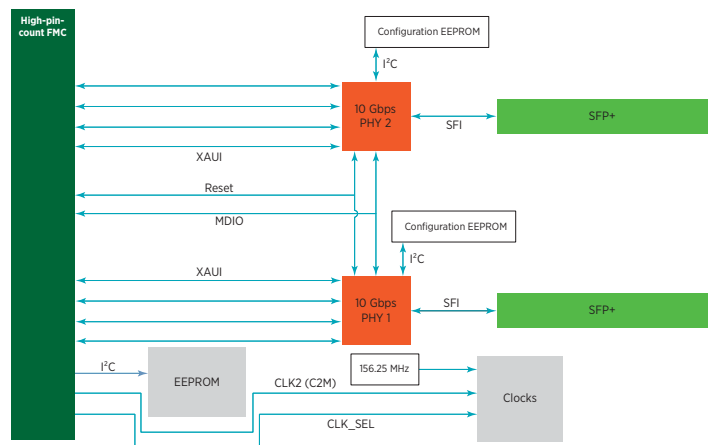
The VITA 57.1 (FMC) standard comes to the rescue of complex designs with its unprecedented mechanical and electrical flexibility – VITA 57.1 provides a standard specification for small mezzanine modules designed to adapt an FPGA-based carrier card to different I/O requirements.

- Supports multiple clock options
- Perfect for Nutaq RD's μ TCA Perseus AMCs

Features

- Two, 10 Gbps PHY transceivers
- PCS, PMA and XGXS sublayers
- XAUI interfaces
- Selectable, onboard clock source:
 - 156.25 MHz (AEL2005s can be used in fiber or copper mode)
 - FMC driven

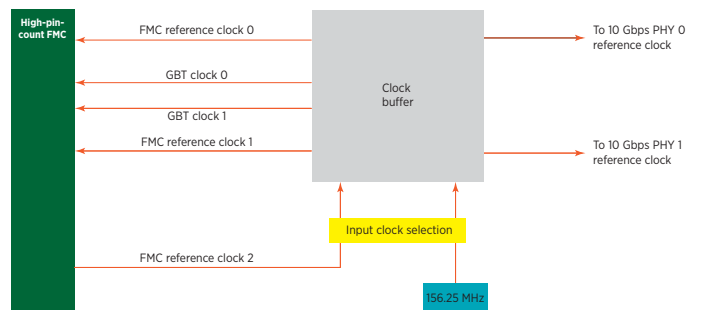
2x10GE SFP+ functional block diagram



Clock management

The module is equipped with an onboard, low-jitter, fixed, 156.25 MHz reference clock or selected from the FMC. The clock is buffered and distributed to both AEL2005s, to both M2C clock outputs, and to GBTCLK0 and GBTCLK1 so as to synchronize the XAUI transceivers. To synchronize several modules, select a user clock with the clock buffer originating from the FMC's CLK2.

2x10GE SFP+ clock modes block diagram



Specifications

FMC connectivity

- High-pin-count connector
 - LA (00-04)
- CLK0 and CLK1 (M2C: selected reference clock)
- CLK2 (C2M: connected to user clock)

Front panel

- 2x SFP+ ports
- 6x LEDs
 - RX
 - TX
 - RX LOS for both channels

Mechanical

- Dimensions: 69 mm × 10 mm × 104 mm (W×H×D)

Standards compliance

- FMC
 - VITA 57.1
- AEL2005 PHY
 - IEEE 802.3ae 10 Gigabit Ethernet
 - IEEE 802.3aq 10 GBASE-LRM
 - INCITS T11 10 Gigabit fiber channel
 - SFP+ MSA 3.0

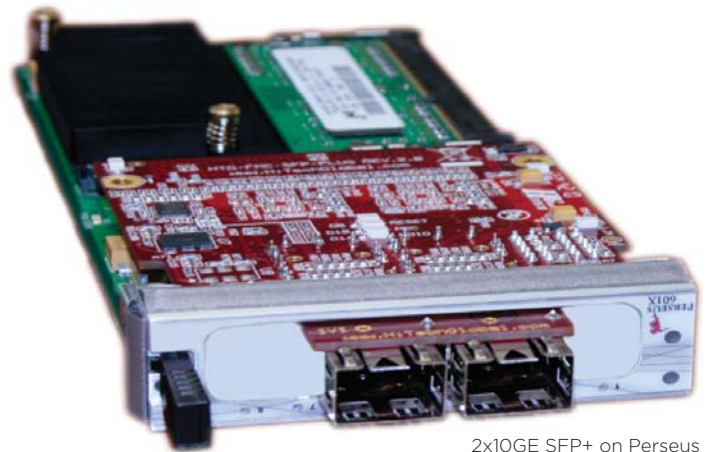
Electrical

- 12 V (unused)
- 3.3 V
- V_{adj} to 2.5 V necessary to power 2x10GE SFP+ logic conversion ICs

Power consumption

- 4.5 W (maximum)

Note: Specifications for the **FMC only**. They do not account for the power consumption of the SFP(+) transceiver module.



2x10GE SFP+ on Perseus

Nutaq products are constantly being improved; therefore, Nutaq reserves itself the right to modify the information herein at any time and without notice. The FMC logo is a trademark of VITA.

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2150 Cyrille-Duquet, Quebec City (Quebec) G1N 2G3 CANADA
T. 418-914-7484 | 1-855-914-7484 | F. 418-914-9477
info@nutaq.com