Nutaq
µSDR420
Massive MIMO Series

PRODUCT SHEET

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µSDR420 Massive MIMO Series

Rapidly design, test, and deploy 100x100 massive MIMO next gen wireless protocols.

Key Benefits

- **Easily migrate from test vector validation to real-time implementation.**
- **Reduce the overall development cycle by 30-60% using included software environment.**
- **Accelerate final product deployment by prototyping on industry standards.**

Key Features

- **Highly efficient bandwidth with low latency throughout the system.**
- **Integrated MicroTCA-based, PCIe switch fabric, 100x100 massive MIMO test bed.**
- **Supports Record/Playback and real-time streaming interfaces.**
- **Includes a MIMO QAM64 OFDM reference design.**
- **Supports both model-based design and GNU Radio.**
- **Provides the RF performance required for next gen advanced waveforms including 4G & 5G.**

Nutaq's µSDR420 Massive MIMO Series addresses the need for rapid design, test, and deployment of massive MIMO-based advanced next generation wireless protocols.

Based on industry standards (MicroTCA, AMC, FMC) the µSDR420 Massive MIMO Series is the only large scale test bed that combines a highly efficient backplane bandwidth, low system latency, and extensive FPGA processing power.

The overall development cycle can be reduced by 30-60% by using the software environment which supports both model-based design and GNU Radio, while the RF aspect provides the performance needed for 4G & 5G development, as demonstrated by the included QAM64 OFDM reference design.

Highlights

System Level

- Scalable to 100x100 RF transceivers & beyond.
- Full BW synchronous record & playback of all channels.
- Timestamp support for accurate time-based control.
- GPS-disciplined (PPS) synchronisation for frequency accuracy.
- Based on industry standards (MicroTCA, AMC, FMC).
- Backplane supplies high speed, low-latency PCIe interconnectivity.
- Simultaneous auto-calibration of all radios.

Hardware Level

- FPGA: Xilinx Virtex-6 based.
- Radio: 28 MHz BW, 300 MHz to 3.8 GHz tuning range.

Software Level

- Rapid prototyping using model-based design tools (GNU Radio, System Generator for DSP).
- QAM64 2x2 MIMO OFDM reference design included.

100x100 Massive MIMO System

In the Nutaq µSDR420 Massive MIMO Series, 100x100 MIMO systems are achieved by combining five 10-slot MicroTCA chassis, with each slot containing a 2x2 radio node, along with a sixth MicroTCA chassis which acts as the PCIe Central Processing Unit.

Hardware Breakdown: 100x100 RF Nodes

- 5x 10-slot MicroTCA chassis.
- 10x FPGA based 2x2 MIMO subsystems in each of the five chassis. Each subsystem consists of:
  - 1x Nutaq's Perseus 601x.
  - 1x Nutaq's Radio420x FMC module in a stacked 2x2 configuration.
- PCIe external fiber/copper QSFP+ cabling to couple to the Central Processing Unit.

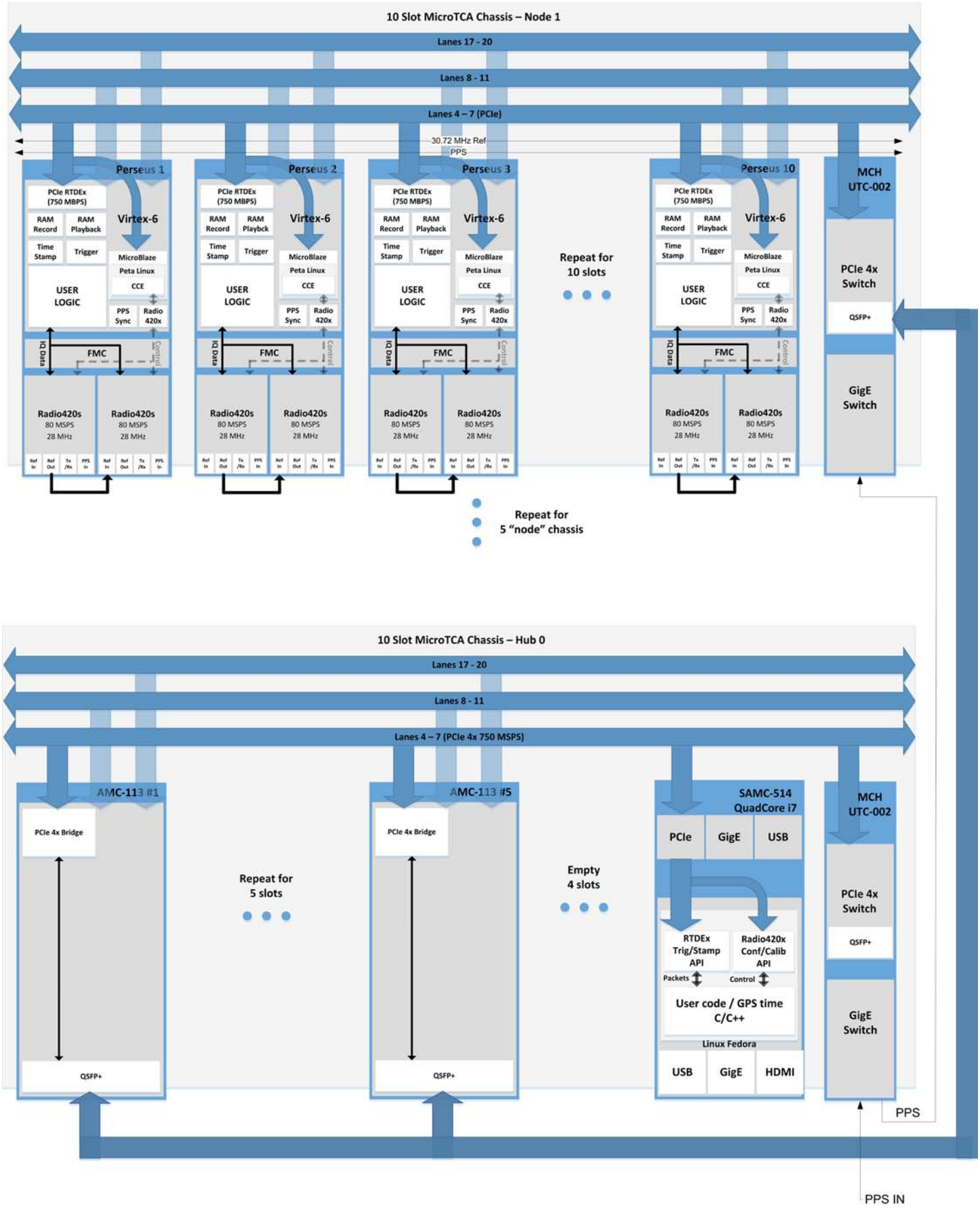
Hardware Breakdown : Central Processing Unit

- 1x 10-slot MicroTCA chassis.
- 5x AMC QSFP+ external cable to PCIe bridge card, linking to the five MicroTCA chassis containing the RF nodes.
- 1x AMC Quad-core i7 CPU blade, as the PCIe root complex and main control unit.
- 4x slots available for user expansion
  - SATA HDD AMCs, IO AMC cards, additional FPGA cards (Perseus 601x), etc.

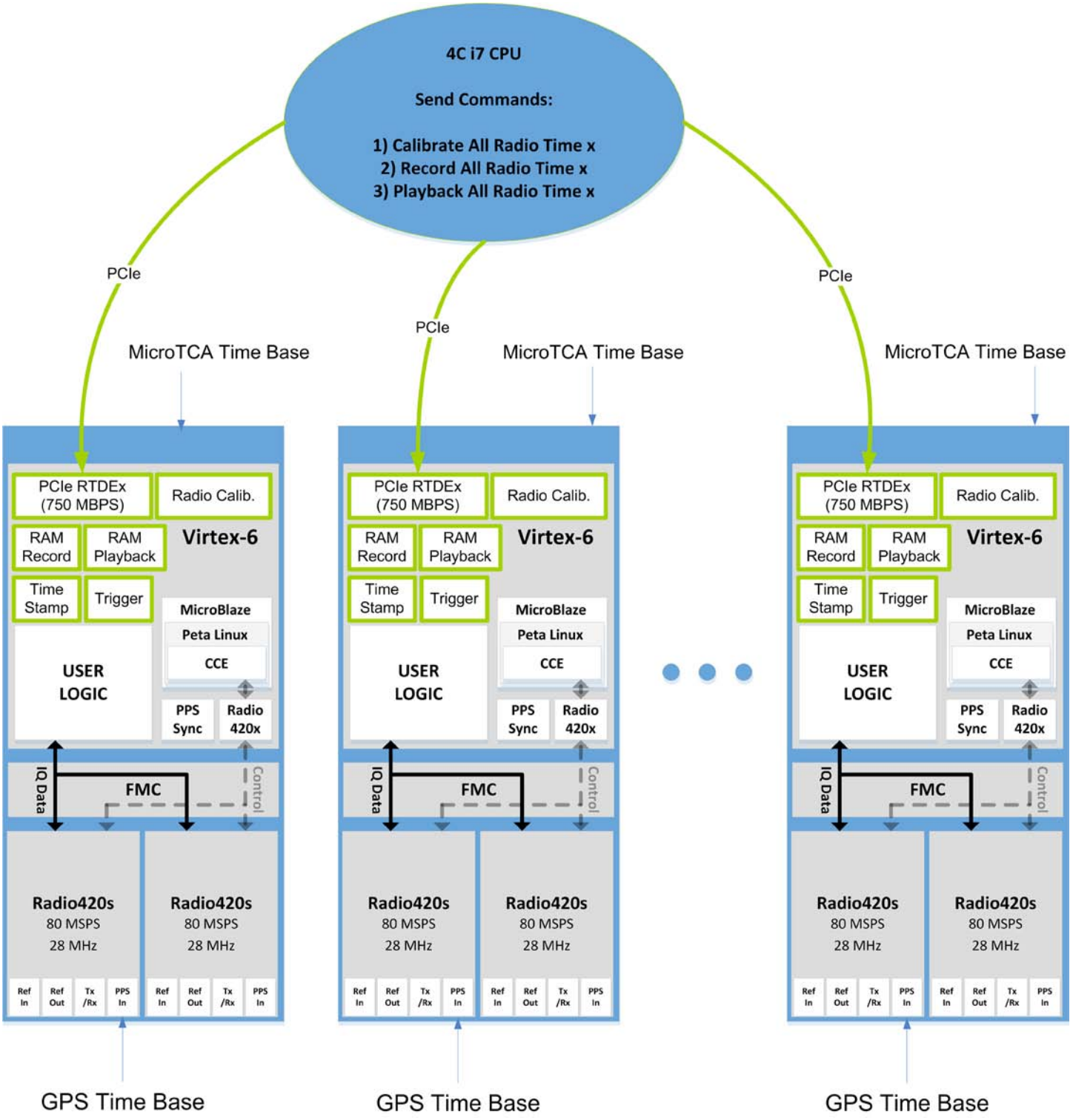
From the Central Processing Unit, each autonomous 2x2 MIMO subsystem can receive time-based commands via Nutaq's included APIs.

This functionality enables numerous massive MIMO development features including:

- 100x RF channel synchronous calibration and programming.
- 100x RF channel synchronous record & playback.
- 100x RF channel synchronous CPU streaming (half-duplex or full-duplex).



100x100 Massive MIMO System



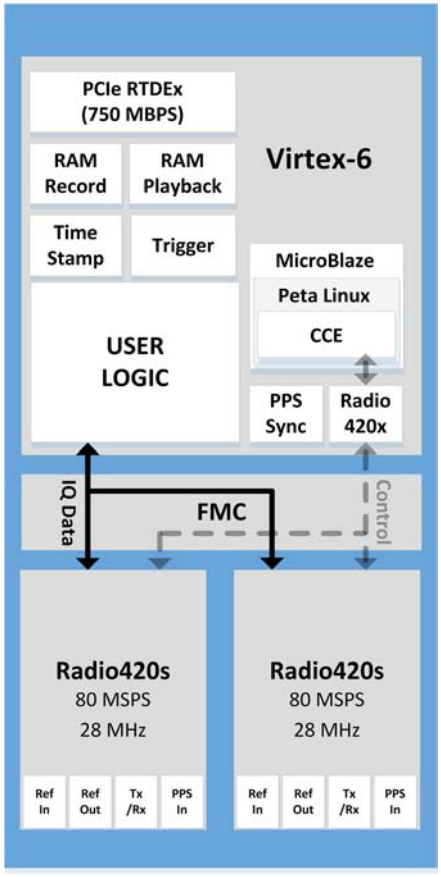
CPU To RF Nodes Synchronous Commands

FPGA Based 2x2 MIMO Subsystem - AMC Perseus 601x With FMC Radio420X

The fundamental unit of the µSDR420 Massive MIMO Series is a 2x2 subsystem which provides the scalability and performance needed to take theoretical techniques from simulation to deployment.

This subsystem consists of an AMC FPGA card (Nutaq's Perseus 601X) combined with a 2x2 MIMO FMC radio card (Nutaq's Radio420x). This subsystem is repeated fifty times to realize the 100x100 massive MIMO solution.

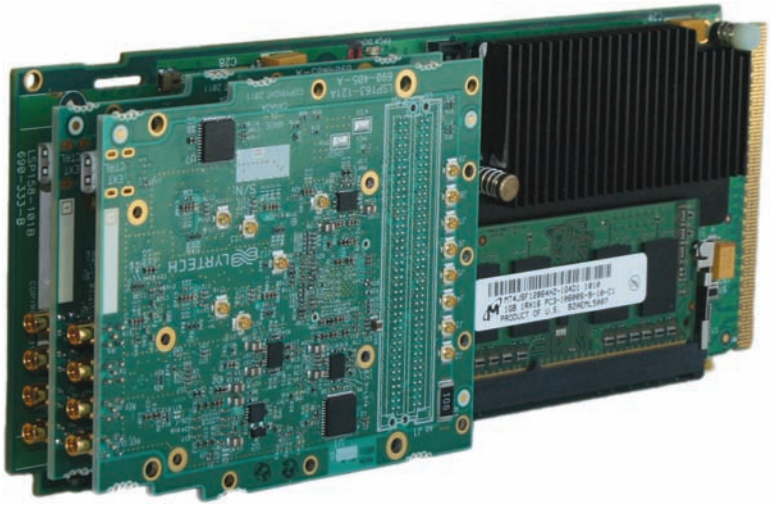
Each subsystem is completely autonomous and comes with various IP cores, while integrating with the software framework.



2x2 MIMO Subsystem

2x2 MIMO Subsystem Features

- Large user logic space for user-based VHDL code implemention.
- Record & playback on a large SDRAM.
- High speed real-time data exchange (RTDEx) through the MicroTCA backplane.
- Board integration to the Simulink environment for user FPGA code implementation.
  - o Model-Based Design using Xilinx System Generator for DSP
- Timestamp functionality.
- Auto-calibration of the 2x2 MIMO RF nodes.
- GPS disciplined radio reference clocks.
- Triggering functionality.
- PCIe for high data throughput with low latency.
- GigE for easy remote network access.
- GNU Radio drivers for rapid prototyping & development on the host.



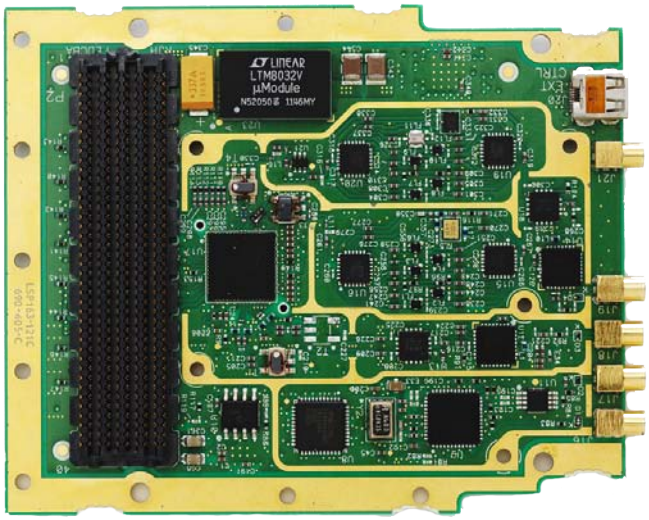
2x2 MIMO Subsystem (Perseus 601X with 2x2 Radio420X)

FMC Radio Cards – Nutaq's Radio420x

Stacked in a 2x2 MIMO configuration, and based on the agile Lime Microsystems LMS6002D RF-IC, Nutaq's Radio420x FMC radio module targets a large range of broadband & narrowband waveforms between 300 MHz and 3.8 GHz.

RF Node Features

- Stackable to 2x2 to reduce deployment costs and footprint.
- Highly shielded, field ready design.
- Tune from 300 MHz to 3.8 GHz.
- Dynamically selectable bandwidth between 1.5 MHz & 28 MHz.
- QAM64 capable for 4G & 5G performance requirements.
- Auto-calibrated radio.
- Low-jitter PLL and 30.72 MHz reference clock.
  - o Also accepts external reference from FPGA carrier card or via front panel connector.
- Internal or external GPS disciplined alignment.



Nutaq's FMC Radio420x

The Full Rate Record/Playback IP Core

Each 2x2 MIMO FPGA-based subsystem is equipped with 4 GB SDRAM FPGA memory, allowing for recording of the full bandwidth:

- Two RF channels @ 80 MSPS = 2 x 160 MBps (2B per sample) = 320 MBps

Thus, the record/playback IP Core enables record or playback of the entire 100x100 system for 1 Gigasample per channel. This translates to 128 seconds for all 100x100 channels at full rate (80 MSPS).

Additionally, multiple operating and trigger modes are available:

Operating Modes

Single Shot:

- Record: Fill up memory, stop, then download data to PC.
- Playback: Upload File, playback from memory.

Normal:

- Record: Fill up memory, stop, download data to PC, then re-arm trigger.
- Playback: Upload file, playback from memory.

Continuous:

Playback: Upload file, playback memory in a continuous loop.

Trigger Modes

External:

- An external trigger for each 2x2 MIMO subsystem is available.

FPGA based:

- The trigger signal can be defined by user logic within the FPGA of each 2x2 MIMO subsystem.

Time-based software:

- The trigger signal can be sent from the central processor unit using time based events.

The Host Streaming Interface – Real Time Data Exchange (RTDEx)

Nutaq's RTDEx IP core provides a framework to exchange data between all 100x100 RF nodes and the central host unit. This is accomplished using PCIe links, yielding the highest bandwidth and lowest latency possible. Additionally, the framework supports remote computer streaming through the use of the Gigabit Ethernet interface.

The 6.4 Gbps PCIe Host BW is shared among all RF nodes (managed via a PCIe central switch), resulting in a channel BW of at least 50 Mbps for each antenna (64 Mbps theoretical).

Typical RTDEx Performance (Obtained Using Linux OS)

Host - FPGA Streaming	GigE	PCIe 4x (Gen 1)
Data BW	1 Gbps	10 Gbsp
Data Throughput	900 Mbps	6.4 Gbps
Roundtrip latency (4 kB, send & receive)	1 msec	200 - 300 µsec

Two RTDEx operating modes are available:

Continuous Mode:

- Minimize latency while maximizing data throughput for sustained streaming data transfer.

Burst Mode:

- Maximize data throughput for a short time period.

The Synchronisation and Time-Based System

Multiple Multiple clock modes are available to ensure all RF nodes within the 100x100 MIMO system are perfectly synchronised. Additionally to ensure no frequency drift in time, multiple GPS-disciplined modes are possible to ensure the frequency is locked at all time.

100x100 RF node synchronisation modes

MCH Backplane Synchronisation

- The MicroTCA carrier hub (MCH) can provide a common 30.72 MHz reference clock to all 2x2 MIMO subsystems. A special clock matrix on the AMC Perseus 601x board allows each Radio420x FMC card to be supplied with a pure, low-jitter clock (avoiding going through the FPGA) whereby each radio PLLs can lock on this common reference.

Front Panel Any Reference Radio420x Synchronisation

- Each 2x2 MIMO subsystem is equipped with an external reference input connector. A multichannel clock generator can then feed any common reference to the fifty individual 2x2 MIMO subsystems.
- Radio420x On Board PLL
    - o Each 2x2 MIMO subsystem is equipped with an onboard 30.72 MHz low jitter reference clock. To ensure perfect synchronization, the GPS-disciplined Nutaq IP Core on each subsystem must be fed a PPS signal via the front panel or from the MTCA backplane.

100x100 GPS-Disciplined Time Base:

- MCH Time-Based Synchronisation
    - o The MicroTCA MCH can send a common PPS to all 2x2 MIMO subsystems, ensuring a common time base to all RF nodes.

- Front Panel PPS Input of Radio420x
    - o Each 2x2 MIMO subsystem is equipped with an external PPS input connector. A multichannel PPS generator can then feed the input of each of the 50 2x2 MIMO subsystems.

Waveform Development Acceleration

Accelerate massive MIMO waveform development and deployment by up to 60% using a model based design approach.

Using a mixed PC-FPGA radio platform which offers complete integration with both GNU Radio and Xilinx System Generator for DSP can radically accelerate advanced massive MIMO wireless waveform deployment.

These sophisticated model-based design tools and automatic code generation tools can eliminate the need for a traditional multi-disciplinary team of algorithm engineers, FPGA engineers, and PC engineers. Instead, the radio waveform can be deployed directly by the algorithm developer, avoiding errors that come from interface interaction and code-translation.

Includes A 2x2 QAM64 OFDM Reference Design

An Alamouti 2x2 QAM64 OFDM reference design implemented in both Simulink (FPGA) and GNU Radio (host) is provided to assist with massive MIMO development.

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2150 Cyrille-Duquet, Quebec City (Quebec) G1N 2G3 CANADA
T. 418-914-7484 | 1-855-914-7484 | F. 418-914-9477
info@nutaq.com