

Nutaq PicoDigitizer-5000

8 channels at 1.25 GSPS or 2 channels at 5 GSPS

PRODUCT SHEET



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Nutaq PicoDigitizer-5000

The PicoDigitizer 5000-Series is a very high speed wideband FPGA-based table top DAQ solution. It incorporates up to 8 channels on a Virtex-6 FPGA, with maximum sampling rates from 5 GSPS (max 2-ch) down to 1.25 GSPS (max 8-ch), and offers an embedded version which includes an Intel Quad-Core i7

Key Features

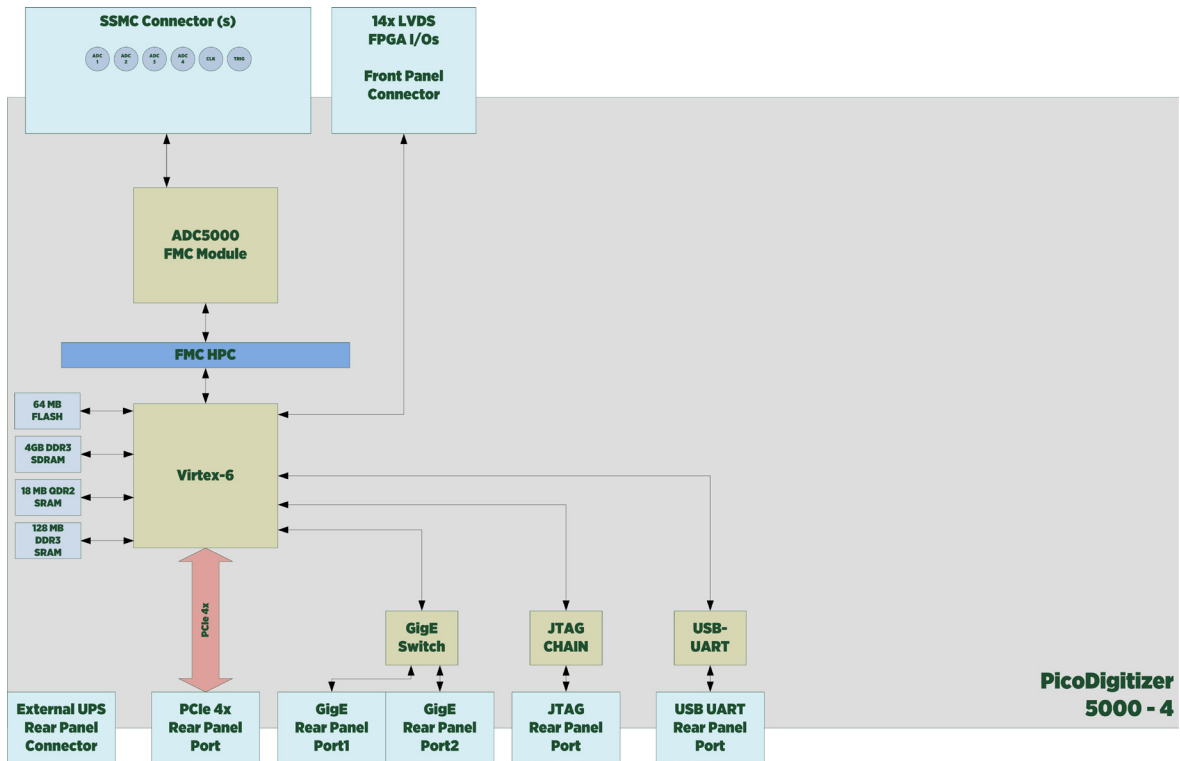
- Up to 8 channels @ 1.25 GSPS, 4 channels @ 2.5 GSPS, or 2 channels @ 5 GSPS
- Large Virtex-6 FPGA(s)
- Optional Intel Quad-Core i7 (embedded version)
- 10 bit resolution
- Onboard/external sampling/reference CLK options
- GigE and PCIe 4x high speed interfaces
- Model-based design integration

Configurations

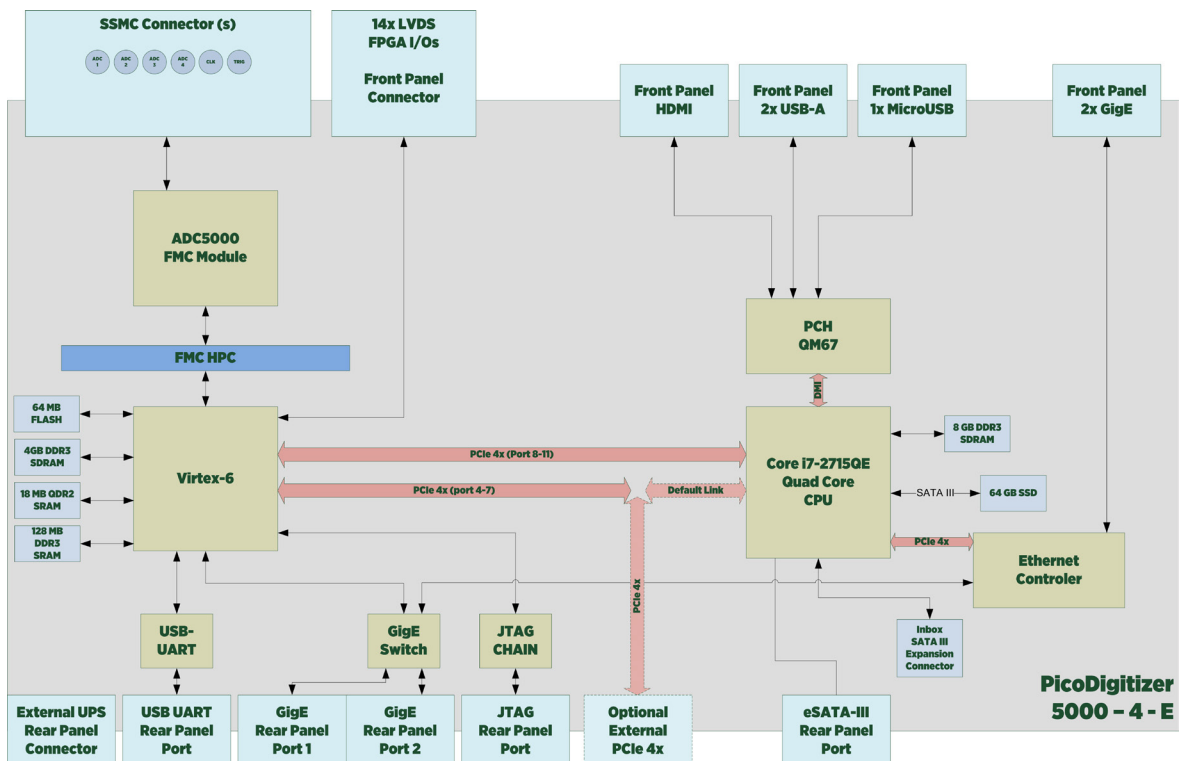
	4 Channel PicoDigitizer-5000	4 Channel PicoDigitizer-5000 (Embedded)	8 Channel PicoDigitizer-5000
Number Of Channels	4	4	8
Maximum Sampling Frequency	5 GSPS (1 ch) 2.5 GSPS (2 ch) 1.25 GSPS (4 ch)	5 GSPS (1 ch) 2.5 GSPS (2 ch) 1.25 GSPS (4 ch)	5 GSPS (2ch) 2.5 GSPS (4 ch) 1.25 GSPS (8 ch)
Resolution	10 bits		
FPGA*	1xVirtex-6		2xVirtex-6
Remote Host Interface	1 x GigE 1 x PCIe-4x	1 x GigE Dual PCIe-4x (Between Virtex-6 & Embedded Quad-Core i7) or Single PCIe-4x (Between Virtex-6 & Embedded Quad-Core i7) & Single PCIe-4x (External)	1 x GigE 1 x PCIe-4x
Embedded CPU	None	Intel Quad-Core i7-2715QE	None
Embedded Storage**	N.A.	64 GB SSD 1x SATA external 1x 200 GB SATA internal (optional)	N.A.

* Virtex-6 options available: LX240T, LX550T, SX315T or SX475T

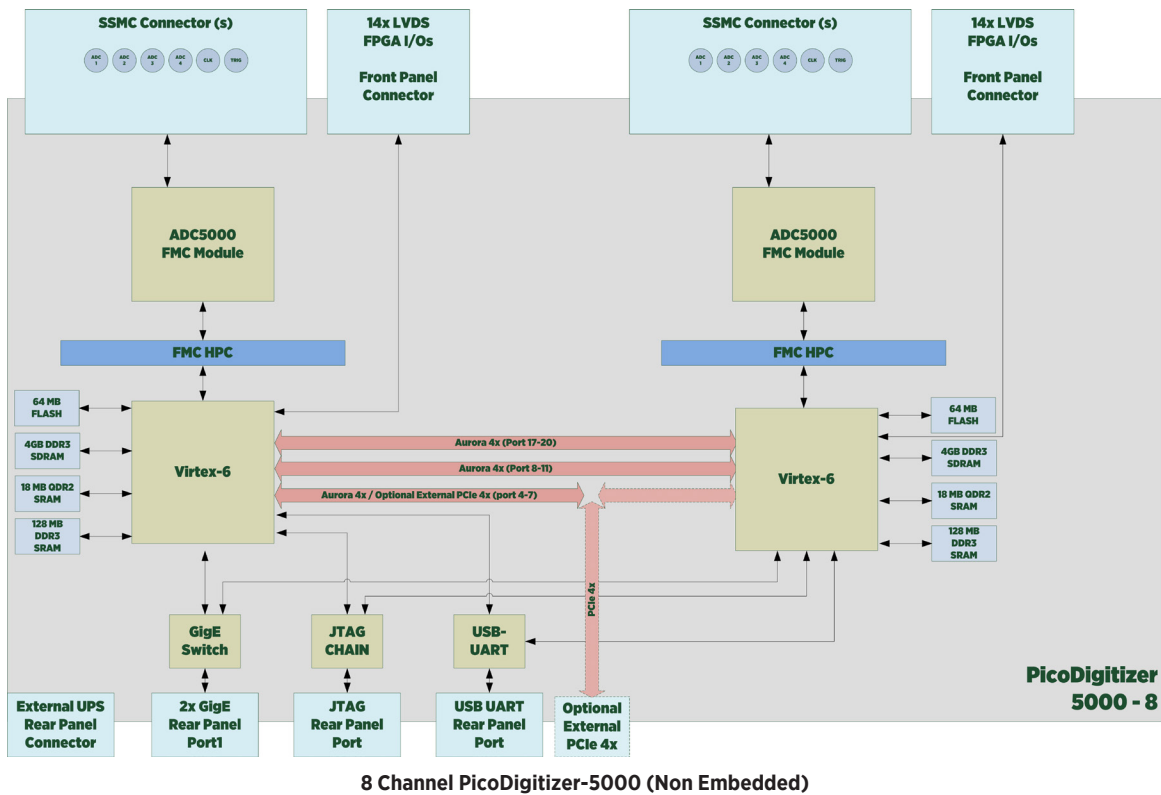
** 1x eSATA connection rear PicoDigitizer panel, 1x SATA for internal 1.8" SSD drive.



4 Channel PicoDigitizer-5000 (Non Embedded)



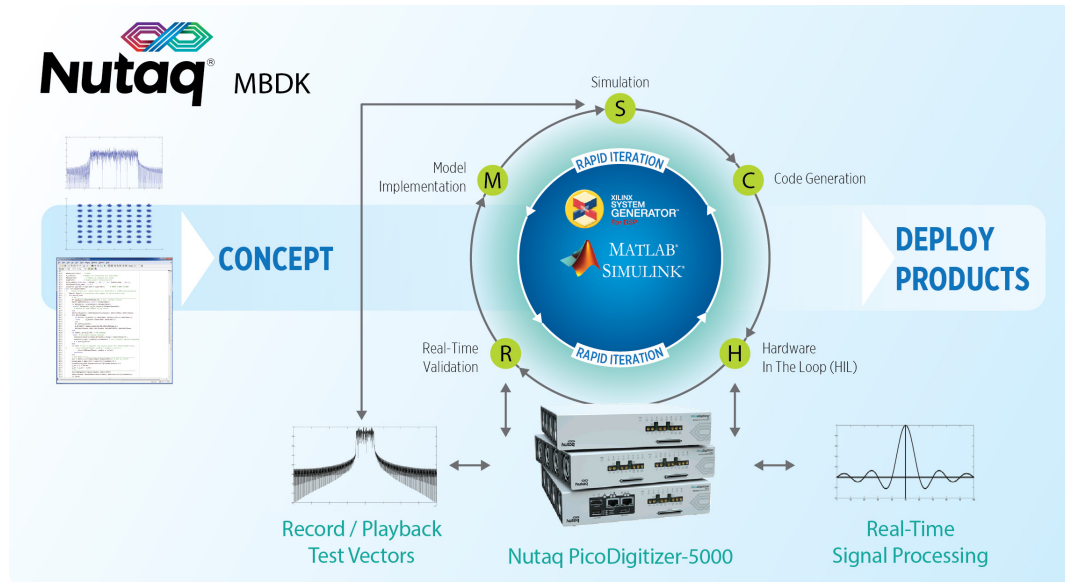
4 Channel PicoDigitizer-5000 (Embedded)



Model-Based Design Flow

Rapid System-Level FPGA Development in MATLAB and Xilinx System Generator for DSP

Built on top of Nutaq's Board Software Development Kit (BSDK), the Model-Based Design Kit (MBDK) enables the rapid design, simulation, testing, and deployment of applications from the Simulink graphical environment without the need for hand-coding in either VHDL or C.



Some of the benefits presented by Nutaq's model-based design approach include:

- A significant reduction in the time spent on low value-added tasks such as programming I/O interfaces, adjusting FPGA constraints, debugging drivers etc.
- Providing host co-simulation tools which enables:
 - o I/O integration within simulations
 - o Step-by-step FPGA fabric design migration
 - o Easy FPGA-to-host interaction
 - o Data logging
- Tools such as record/playback, host I/O control, and data streaming libraries.

FPGA Recording Core

The FPGA recording IP core enables storage of very high speed multichannel bursts of data in the FPGA-attached SDRAM. This data can then be transferred to a host device for storage and/or real-time analysis.

The FPGA recording IP core comes with standard trigger mechanisms (single shot, normal, software-defined). The trigger sources can either come from the host processor, a user defined FPGA signal, or from the PicoDigitizer-5000 Series trigger front panel input.

The user can define the number of channels to record, as well as the acquisition rate so that the available recording memory bandwidth is efficiently used.

Note that FPGA preprocessing on the channels can be performed before recording to potentially reduce recording bandwidth needs.

- DDR3 FPGA memory size = 4 GB
- Maximum data throughput = 5.7 GBps
- Maximum number of channels recorded at 5 GSPS per FPGA node = 1x (5000 MHz, 1 bit per sample: truncated on 8-bit)
- Maximum number of channels recorded at 2.5 GSPS per FPGA node = 1x (2500 MHz, 2 bits per sample: 10-bit extended on 16-bit)
- Maximum number of channels recorded at 2.5 GSPS per FPGA node = 2x (2500 MHz, 1 bit per sample: truncated on 8-bit)
- Maximum number of channels recorded at 1.25 GSPS per FPGA node = 2x (2500 MHz, 2 bits per sample: 10-bit extended on 16-bit)
- Maximum number of channels recorded at 1.25 GSPS per FPGA node = 4x (2500 MHz, 1 bit per sample: truncated on 8-bit)

Application Example

- FPGA-based filtering on 4 channels sampled at 1.25 GSPS on the FPGA (decimation by 16 through FIR filters), then recording of all channels. Each channel can be recorded for 6.4 seconds.

RTDEx (Real-Time Data Exchange)

Nutaq's RTDEx IP core provides users with a framework to exchange data with a host device through either the GigE or PCIe links, yielding the highest bandwidth and lowest possible latency.

Built to complement our "snapshot" FPGA recording capabilities, the RTDEx IP core provides a continuous data flow from the FPGA to the host computer, for further real-time computing or real-time PC recording.

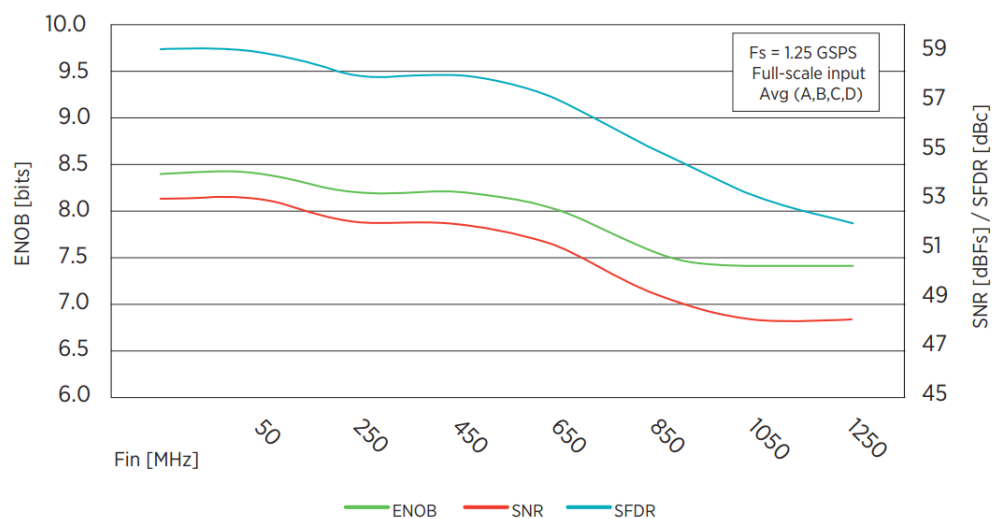
HOST - FPGA Streaming	GigE	Dual PCIe 4x
Data BW	1 Gbps	20 Gbps
Data Throughput	900 Mbps	12.8 Gbps
Roundtrip Latency (4 kB, send & receive)	1 msec	200-300 µsec

Specifications

FPGA(s)	
	Supports LX240T, LX550T, SX315T and SX475T FPGA devices
	Supports up to 2 PCIe (4x) interfaces; Supports GigE interface
	4 GB SODIMM DDR3
	18 MB QDR2 SRAM
	64 MB NOR Flash
Embedded CPU	
	Intel Quad-core i7 Gen2 CPU, 2.1 GHz processor
	8 GB DDR3 SDRAM
	64 GB SSD +1x SATA external +1x 200 GB internal (optional)
	GigE & Dual PCIe 4x support
	SATA -II/III support
	Embedded throughput (FPGA-CPU) : 1x PCIe 4x - 6 Gbps or 2x PCIe 4x
A/Ds	
Sampling Rate, Resolution	Up to 5 GSPS, 10 bits
Number of channels	Up to 8 channels
Clock	
	Onboard PLL or external sampling CLK input
Reference Clock	
	Onboard or external input

Performance

- 500 mV_{pp} analog input range
- Selectable input bandwidth (1 GHz or 3 GHz)
- Individual gain control (310%)
- Individual offset control (340 mV)
- Individual phase control (315 ps)
- > 60 dB channel isolation (crosstalk)



Front Panel Connectors

Analog Inputs, CLK & Triggers

(All PicoDigitizer 5000-Series Models)

For each FPGA digitizer node

- 4 x A/D SSMC inputs
- 1 x external trigger input
- 1 x external sampling or reference CLK input

Digital Inputs & Outputs

(All PicoDigitizer 5000-Series Models)

For each FPGA digitizer node

- 1x VHDCI connector

VHDCI Connector Signal Map

- 14 x user LVDS I/O data
- 1 x LVDS clock

Additional Front Panel Connectors

(PicoDigitizer 5000-Series 4x Channel

Digitizer Node, Embedded Version Only)

- 1 x HDMI
- 2 x GigE
- 1 x Mini USB port
- 1 x COM-port
- 1 x USB 2.0 ports

Rear Panel Connectors

- 2x GigE ports
- 1x USB UART FPGA console port
- 1x external universal power supply
- 1x eSATA (Embedded models only)
- 1x PCIe 4x cable interface connector

Ordering Information

PicoDigitizer5000-A-B-C-D-E

A (Embedded CPU)	0 = No embedded CPU	1 = Embedded CPU
B (FPGA Option)	0 = LX240T	1 = LX550T
	2 = SX315T	3 = SX475T
C (# of A/D channels)	0 = Up to 4 channels	1 = Up to 8 channels
D (External PCIe)	0 = No external PCIe	1 = PCIe 4x external link to FPGA
E (Model Based Design Software License)	0 = No software license	1 = 1x MBDK Workstation License
F (Model Based Design Software License)	0 = No software license	1 = 1x MBDK Workstation License

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